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Low Power High Speed with Improved Noise Margin for Domino CMOS Inverter.

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ABSTRACT

Employment and income play an integral role in ensuring livelihood security of fishermen. SHGs and co-operatives in various fishing villages are functioning as an effective mechanism for overcoming the livelihood insecurity prevailing at present in the fishing sector of Kerala. 900 samples have been collected from the fishery related SHGs and co-operatives from twelve fishing villages of six districts coming under three zones based on number of SHGs and number of fishing crafts and gears used. The results obtained from the study show that their income from fishing and non fishing activities works as a reinforcing factor for their socio-economic development. Even though the fishermen community has benefitted from the new institution set up, they still remain as outliers in the state requires requisite policy framework for the overall development of the fishing community of Kerala.

Keywords : Body biasing, Noise immunity, AVL circuit technique, CMOS

INTRODUCTION

Today, the necessity of portable systems and simultaneously improvement in battery performance depicts that power consumption is major factor in CMOS VLSI design parameters [3]. To reduce dynamic power dissipation it is necessary to reduce the supply voltage of the circuit, reduction of supply voltage after a certain limit affects the performance of the circuit, to maintain circuit performance of the circuit it is necessary to decrease the threshold voltage as well, but it leads to leakage power dissipation. Leakage power can be reduced by increasing the threshold voltage [5]. In this paper to reduce the voltage applying to the load circuit, we suggest the use of AVL (Adaptive Voltage Level) circuit technique. AVL circuit is controlled by sleep control signal, which increases the noise immunity. The advantage of using AVL circuit is that the load circuits can operate quickly when they are in active mode due to the increase in drain-source current as the AVL circuit supplies the maximum drain-source voltage V_{ds} to the on-MOSFETS through on-switches. On the other hand, during standby mode, it supplies a slightly lower voltage through the weakly-on switches [2]. Hence the sub-threshold leakage current of the off-MOS transistors decreases and the standby power gets reduced. It also produces high noise immunity. When we applied voltage to the substrate of a MOSFET it affects the threshold voltage of a MOSFET as well. The voltage difference between the source and the substrate, VBS also affects the width of the depletion layer and due to changes in the charge in depletion layer voltage across the oxide also get changed. Therefore the expression for the threshold voltage is given by:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_F + V_{SB})}}{C_{ox}}$$

The threshold difference due to an applied source-substrate voltage can therefore be expressed by:

$$\Delta V_T = \gamma(\sqrt{(2\phi_F + V_{SB})} - \sqrt{2\phi_F})$$

Where γ is the body effect parameter given by:

$$\gamma = \frac{\sqrt{2\varepsilon_s q N_a}}{C_{ox}}$$

Substrate biasing provides an effective circuit-level technique for varying threshold voltage and to enhance the performance of the circuit.

This paper gives emphasis on high speed and low power design as well as improved noise margin for domino inverter technique. Among different dynamic logic circuit techniques, domino logic technique is mostly used because it provides less delay and its area consideration, but it has less tolerance to noise and its static power consumption is high. So in this paper we have applied AVL circuit technique and body bias technique to overcome both of these problems

STANDARD DOMINO INVERTER

A standard domino inverter is as shown in Figure 1. A standard Domino inverter consists of an n-type dynamic logic block followed by a static inverter. During pre-charge phase the output node of the dynamic CMOS stage is pre-charged to high logic level and the output of the inverter becomes low [4]. During evaluation phase, the output node of the dynamic CMOS stage is either discharged to a low level or it remains high. Consequently the inverter output voltage can also make at most one transition during the evaluation phase from 0 to 1. If the output of the domino gate is applying to other domino gates, then it is necessary that all input logics are set to 0 at the end of the pre-charge phase and the transitions during evaluation are only 0 to 1. Hence the dynamic node discharges only when the previous stage evaluates to 1 and due to the static inverter at the output, we get high fan-out.

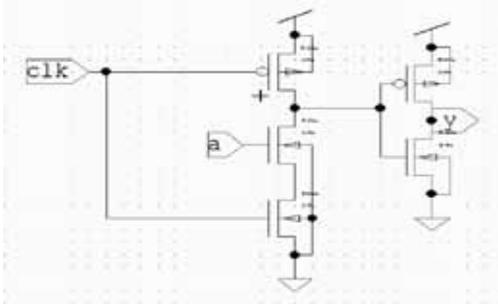


Figure 1 Domino Inverter

AVL INVERTER

In this circuit AVL circuit is connected above the Domino Inverter. AVL circuit contained one p-MOSFET and two series connected n-MOSFETS, which will reduce the voltage applying to the load circuit. AVL circuit is controlled by sleep (slp) control signal [1]. When sleep signal is low, the p-MOSFET is on, while series connected n-MOSFETS are off. During this operation, we get the full voltage out of the AVL circuit. When sleep signal make transition from low to high, this will turn-on series connected n-MOSFETS, and turn-off p-MOSFET, Thus, the drain-to-source voltage (Vdsn), of the off n-MOS in load circuit (domino inverter) can be expressed as

$$V_{dsn} = V_{DD} - 2v$$

Where v is a voltage drop of the series connected single n-MOSFET and Vdsn can be changed by changing the number of series connected n-MOSFETS. If Vdsn decreases this will increase the barrier height of the off n-MOS [6], therefore it will decrease the drain induced- barrier-lowering (DIBL) effect and, consequently, increase Vth. This results in a decrease in the sub threshold current of the n-MOS, therefore the leakage current through the inverter decreases.

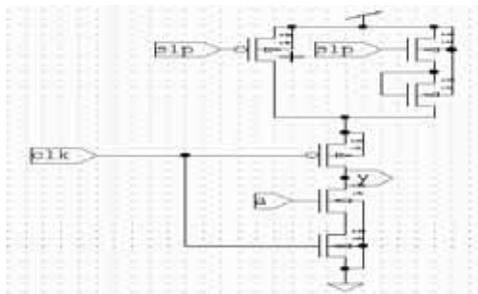


Figure 2 AVL Inverter

BODY BIAS INVERTER

Domino logic gates are frequently employed in high performance circuits for high speed and area efficiency. As supply voltage is reduced, delay increases, unless threshold voltage Vth is also decreased. Substrate biasing provides an effective circuit-level technique for varying threshold voltage. Here substrate of NMOS and PMOS is connected to clock, which increases the threshold voltage that in turn reduces the leakage current.

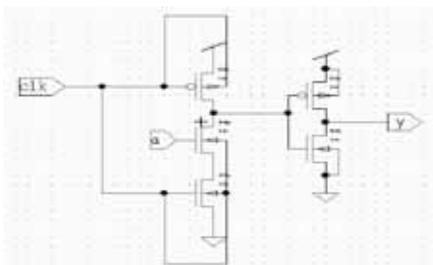


Figure 3.Body Bias Inverter

INVERTER USING PROPOSED TECHNIQUE

In the proposed method to reduce the delay, and power dissipation as well as to improve the noise margin we have used Body biasing technique with AVL circuit technique. In this method we have taken Domino Inverter with AVL circuit and body biasing. Here the substrate of PMOS and NMOS is connected to the clock. The simulations are performed using Tanner EDA Tools 180 nm technology. It is beneficial to use AVL circuit technique with load circuit because, the load circuit will operate very fast when they are in active mode due to increase in drain source current but in stand by mode due to less drain source voltage, threshold voltage will increase which reduces the leakage current, of the circuit [1].

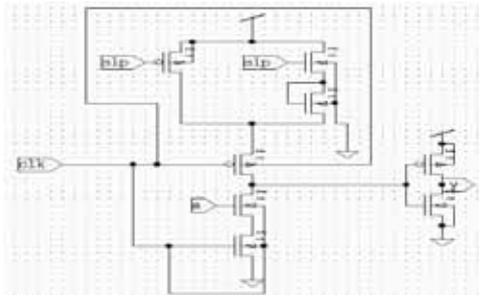


Figure 4.Proposed Inverter

PARAMETERS OBSERVATION

The parameters observations of different techniques are as follow:

| Technique | Dynamic power dissipation In mili watts | Leakage Power in nano watts | Evaluation Delay in Pico seconds | Noise margin in volts (NMH) | Noise margin in volts (NML) |
|--------------------|---|-----------------------------|----------------------------------|-----------------------------|-----------------------------|
| Domino Inverter | 0.483 | 0.049 | 19.48 | 1 | 1 |
| AVL Inverter | 0.796 | 0.224 | 22.62 | 1.5 | 1.45 |
| Body Bias Inverter | 789.58 | 0.051 | 12.90 | 3 | 1.5 |
| Proposed inverter | 14.34 | 0.123 | 12.79 | 3 | 1.5 |

Table 1.Parameters observation

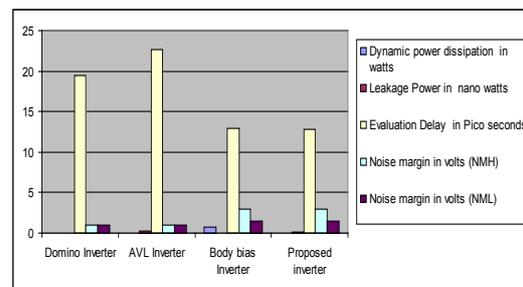


Figure 5. Comparison of power consumption, delay and noise margin

SIMULATION RESULTS

The output of the domino inverter is shown below



Figure 6 Domino Inverter

The output of the AVL inverter is shown below

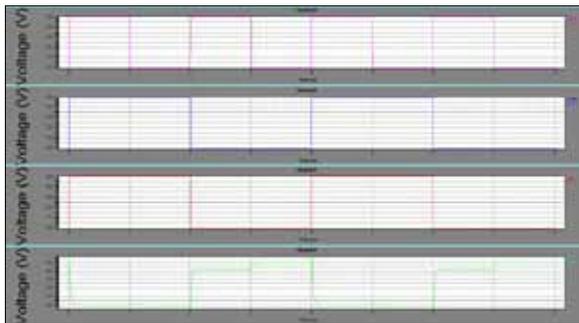


Figure 6.AVL Inverter

The output of the body bias inverter is shown below

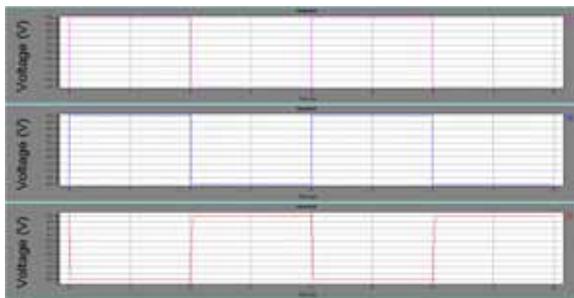


Figure 7.Body bias Inverter

The output of the proposed inverter is shown below



Figure 8.Proposed Inverter

CONCLUSION

In this paper we have designed Domino inverter with AVL circuit and body bias techniques, and compared it with standard domino inverter, AVL inverter and body bias inverter. Simulation results shows that AVL inverter has more evaluation delay and leakage power dissipation than other techniques and it has less noise immunity. Body bias inverter shows high noise immunity and delay is less than Domino inverter and AVL inverter techniques, leakage power dissipation is also less but it shows very high dynamic power dissipation.

In this dissertation we can say that our proposed inverter is high speed as well as better in noisy environment.

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